REMARKS

Claims 1-5 were originally presented for examination in the present Application. In the aforementioned Office Action, the Examiner rejected claims 1-5 as being anticipated under 35 U.S.C. §102 by either U.S. Patent Application Publication No. US2001/0047509 by Mason et al. (hereinafter "Mason") or U.S. Pat. No. 6,052,773 to DeHon et al. (hereinafter "DeHon"). The Examiner also objected to wording in claim 5. By this communication, claims 2, 3 and 5 have been amended, and new claims 6-18 have been added. Claims 1-18 are currently pending in the Application. Applicants respectfully request reconsideration of the Application in view of the foregoing amendments and the remarks set forth below.

OBJECTION TO CLAIM 5

The Examiner objected to the phrase "a programmable logic adapted" in claim 5 as being unclear. Applicants have amended claim 5 to recite "a programmable logic core adapter." The programmable logic core (PLC) adapter element is described in the specification at, inter alia, page 7, line 20 to page 8, line 2. Applicants request withdrawal of the objection in view of the amendment.

REJECTIONS UNDER 35 U.S.C. § 102

1. Rejections Based on Mason

Claims 1-3 were rejected under 35 U.S.C. 102(e) as being anticipated by Mason. Applicants respectfully traverse these rejections.

In support of these rejections, the Examiner relied on page 3, paragraph 0057 of Mason for the teachings of "identifying a programmable logic core," "identifying an application," and "designing an application specific circuit for the application" in claim 1; "identifying a programmable logic core for the integrated circuit" in claims 2 and 3, and; "establishing a sign-off design associated with the programmable logic core" in claim 3. The cited section, which is included in a list of definitions extending from paragraph 0043 to paragraph 0073 of Mason, states:

> [0057] IOB: input/output block, a basic building block on a programmable logic device for providing an interface between circuits on the device and external devices/systems; an illustrative IOB is described in the "1999 Programmable Logic Data Book", published by Xilinx, Inc, pages 3-5 to 3-7.

Applicants respectfully submit that the relied upon section, which constitutes a bare definition of an input/output block, fails to teach any of the claim elements of "***identifying*** a programmable logic core" (emphasis added), "***identifying*** an ***application***" (emphasis added), "***designing*** an ***application specific circuit for the application***" (emphasis added), or "***establishing*** a ***sign-off design associated*** with the programmable logic core" (emphasis added), and that claims 1-3 are therefore not anticipated by Mason.

Regarding claim 1, the Examiner relied upon paragraph 0016 of Mason for the teaching of the limitation of "integrating the programmable logic core into the designed application specific circuit." This paragraph discusses dividing the top level design into modules and determining their size and location on the PLD chip. This step is performed prior to actually programming the PLD by storing the instruction sets associated with each module in the location designated for that module on the PLD, which is not "integrating" a "programmable logic core" into an ASIC. The Applicants respectfully submit that it is not clear how "merging constraints from one file to another file" is related to integrating a programmable logic core into an ASIC. Paragraph 0016 does not even mention a core or an ASIC, and does not discuss a step of "integrating."

Regarding claims 2 and 3, the Examiner cited paragraph 0027 of Mason for the teaching of the limitations of "controlling the design of application specific circuit ... in accordance with the set of timing constraints" in claim 2, and of "controlling the design of application specific circuit...in accordance with the sign-off design" in claim 3. However, a close reading of Mason reveals that paragraph 0027 is immediately preceded by the title "Assembly Phase" (paragraph 0026), clearly indicating that the paragraph 0026 discusses the assembly of the device that is under discussion, rather than a process of "controlling the design," as recited in claims 2 and 3. Further, paragraph 0027 does not mention an "application specific circuit," recited in the passage above and in claims 2 and 3, and does not mention the "sign-off design" in the passage referred to above and in claim 3. Therefore, the Applicants respectfully submit that it is not clear how paragraph 0027 can teach controlling the design of an application specific circuit in accordance with a timing constraint or a sign-off design as recited in claims 2 and 3, respectively.

Further in regard to claims 2 and 3, the Examiner relied upon paragraph 0082 of Mason for the teaching of the aforementioned limitations of "controlling the design of application specific circuit ... in accordance with the set of timing constraints" in claim 2, and of "controlling the design of application specific circuit...in accordance with the sign-off design" in

claim 3. A close reading of the cited paragraph reveals that it is directed to partitioning a PLD so that different people work can work on different modules that are programmed into the PLD. In contradistinction to this teaching, the claim limitations involve controlling of the **design** of an ASIC.

Moreover, Applicants note the problem addressed by Mason is that of partitioning a PLD, which is not an ASIC and does not normally contain an ASIC. The Examiner has not shown any disclosure of an ASIC in combination with the PLD taught by Mason. In contradistinction, claims 1-3 of the present Application specify an ASIC.

In sum, Applicants submit that each of claims 1-3 of the Application, as amended by this communication, recites multiple limitations that are neither disclosed nor suggested by Mason, and that the rejection of these claims based on anticipation by Mason should be withdrawn.

2. Rejections Based on DeHon

The Examiner rejected claims 4 and 5 under 35 U.S.C. § 102(b) as being anticipated by DeHon. Applicants respectfully traverse these rejections.

Regarding claim 4, the Examiner relied upon column 3, lines 59-63 of DeHon for the teaching of "a programmable logic core," and upon column 2, lines 59-67 of DeHon for the teaching of "application specific circuitry...being designed in accordance with a sign-off design." However, a close reading of DeHon indicates that these sections refer to two separate and distinct embodiments of the DeHon invention. More specifically, the text of column 3, lines 59-63, corresponds to a first embodiment of the invention (identified under the heading "Configurable Logic as attached logic or function unit" at column 5, line 33 of DeHon), which is depicted in FIGS. 1 and 1A-1H and described more fully at column 5, line 34 to column 10, line 67). In contrast, the text of column 2, lines 59-67, corresponds to a second embodiment (identified under the heading "Configurable logic as control logic" at column 11, line 1), separate and distinct from the first embodiment, which is depicted in FIGS. 2 and 2A-2F and described more fully at column 11, line 2 to column 15, line 33. Applicants submit that the Examiner's rejection is based on an improper combination of elements from two separate and distinct embodiments of the invention embodied by DeHon. Since anticipation under §102 requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984)), the Examiner cannot maintain a §102 rejection based

on the presence of a first claim limitation (i.e., the programmable logic core) in the first embodiment of DeHon and the presence of a second claim limitation (i.e., application specific circuitry) in the second embodiment of DeHon. Furthermore, since no apparent motivation exists to combine the teachings of the two embodiments, claim 4 is submitted to be patentable over DeHon. Withdrawal of this rejection is thus believed to be in order.

Regarding claim 5, Applicants submit that the §102 rejection based on DeHon is improper for substantially the same reasons set forth above in connection with claim 4. More specifically, the Examiner's rejection relies on the combination of teachings of two separate and distinct embodiments for anticipation of the "programmable multi-scale array" and "application circuit interface" limitations. Since this combination is neither taught nor suggested by DeHon, claim 5 is patentable thereover.

Further in regard to claim 5, although column 3, lines 59-63 (cited by the Examiner), teaches PFU 514, the Applicants respectfully submit that there is no disclosure in column 3, lines 59-63, that PFU 514 can handle multiple scales, and the Applicants respectfully submit that there is no other disclosure of a multi scale array in column 3, lines 59-63.

New Claims

New claims 6, 7, and 17 recite details of the programmable multi-scale array to better define the claimed integrated circuit over the prior art. New claims 8 and 17 recite the programmable logic core control to better define over DeHon. New claims 9 and 17 recite the scratchpad memory to better define over DeHon. New claims 10 and 17 recite the configuration test interface to better define over DeHon. New claim 11 recites the microprocessor core to better define over DeHon. New claim 12 recites functions associated with blocks (e.g., perimeter blocks) of the programmable logic core to better define over DeHon. New claim 13 recites the structure of the arithmetic logic unit of the programmable logic core to better define over DeHon. New claim 14 recites an IP core connected to the arithmetic logic units of the programmable logic core to better define over DeHon. New claim 15 recites the states associated with the programmable logic core to better define over DeHon. New claim 16 is similar to claim 4 except that claim 16 is in means plus function format. New claim 17 recites the overall construction of the integrated circuit, which is very different than DeHon. New claim 18 recites a portion of the program flow of FIG. 7 and, among other things, recites a data associated with a multi-scale array not present in DeHon.

CONCLUSION

Therefore, in view of the above remarks this application is in condition for allowance, and the Examiner is respectfully requested to allow this application. The Examiner is invited to contact Applicants' undersigned representative regarding any issues that the Examiner feels are still outstanding.

Respectfully submitted,

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AMENDMENT SHOWING CHANGES FROM PREVIOUS VERSION

In the Specification:

Replace the paragraph bridging pages 5 and 6 with the paragraph below.

The Programmable Logic Core (PLC) is a very high density, high-speed configurable logic structure for use in the development of ASIC components. As illustrated in FIG. 2, the PLC is based on an array of Configurable Arithmetic Logic Units (CALUs) called the Multi-Scale Array (MSA). This structure directly supports **functions of different scales, such as** Register Transfer Level (RTL) functions [~~such as~~]**(e.g.,** counters and adders**)** as well as complex state machine and random logic structures. Scratchpad memory blocks may be incorporated into a specific PLC Core to supplement the internal register storage capabilities of the MSA for datapath intensive applications. The Application Circuit Interface (ACI) provides the signal interface between the MSA programmable routing resources and the application circuitry. The ACI is optimized for each PLC Core and includes scan test registers which allow effective testing of the PLC independent of the application specific circuits, testing of the application specific circuits independent of the PLC and concurrent testing of the combined PLC and application specific circuit behavior. The PLC Control block provides control mechanisms for loading configuration data into the MSA, controlling the application clock and reset signals and for testing the PLC blocks.

Replace the full paragraph in the middle of page 6 with the paragraph below.

The MSA can be implemented, for example, by the techniques disclosed in co-pending U.S. Appln. No. 09/475,400, commonly owned by the assignee of the present invention, the contents of which are incorporated fully herein by reference. Although an MSA based on the principles of **the** co-pending application is considered preferable, the present invention is not limited thereto, and those skilled in the art will be able to underst[~~oo~~]**an**d how to extend the principles of the invention to other types of programmable logic structures after being taught by the present disclosure.

In the claims:

1. (Original) A method of designing an integrated circuit, comprising:

identifying a programmable logic core;

identifying an application;

designing an application specific circuit for the application; and

integrating the programmable logic core into the designed application specific circuit.

2. (Currently Amended) A method of designing an integrated circuit, comprising:

identifying a programmable logic core for the integrated circuit;

establishing a set of timing constraints associated with the programmable logic core; and

controlling the design of application specific circuitry that interfaces with the programmable logic core in the integrated circuit in accordance with the set of timing constraints.

3. (Currently Amended) A method of designing an integrated circuit, comprising:

identifying a programmable logic core for the integrated circuit;

establishing a sign-off design associated with the programmable logic core; and

controlling the design of application specific circuitry that interfaces with the programmable logic core in the integrated circuit in accordance with the sign-off design.

4. (Original) An integrated circuit, comprising;

a programmable logic core; and

application specific circuitry, the application specific circuitry being designed in accordance with a sign-off design.

5. (Currently amended) An integrated circuit according to claim 4, wherein the programmable logic core includes:

a programmable multi-scale array;

an application circuit interface for providing a signal interface between the programmable multi-scale array and the application specific circuitry; and

a programmable logic core adapte[d]r that configures the programmable multi-scale array.

6. (New) The integrated circuit of claim 5, wherein the programmable multi-scale array comprises an array of configurable arithmetic logic units supporting at least:

register transfer level functions; and

random logic structures.

7. (New) The integrated circuit according to claim 4, wherein the programmable logic core comprises a programmable multi-scale array supporting functions of different scales.

8. (New) The integrated circuit according to claim 4, wherein the programmable logic core includes at a programmable logic core control for loading configuration data into the programmable logic core.

9. (New) The integrated circuit according to claim 4, wherein the programmable logic core comprises:

an array of configurable logic structures having internal storage registers; and

a scratchpad memory to supplement the storage registers.

10. (New) The integrated circuit according to claim 4, wherein the programmable logic core includes at a configuration test interface for data and control flow between the application specific circuit and the programmable logic core.

11. (New) The integrated circuit according to claim 4 further comprising a microprocessor core communicatively connected to the programmable logic core.

12. (New) The integrated circuit according to claim 4, wherein the programmable logic core comprises blocks supporting:

configuration data control logic;

scan path logic; and

application circuit interface logic.

13. (New) The integrated circuit according to claim 4, wherein the programmable logic core comprises arithmetic logic units including:

function cells; and

an arithmetic logic unit controller.

14. (New) The integrated circuit according to claim 4, wherein the programmable logic comprises:

an internet protocol core; and

arithmetic logic units communicatively connected to the internet protocol core.

15. (New) The integrated circuit according to claim 4, wherein the programmable logic core supporting:

an idle state that is entered after an assertion of a signal that power is good;

a built in self test state for testing the programmable logic core, the built in self test state is entered from the idle state upon receipt of a test command;

a configuration state for implementing a configuration process, the configuration state supports entry from the idle state and from the built in self test state after receipt of a configuration clock signal; and

an operate state that controls operations of arithmetic logic units, and is entered after completion of the configuration process.

16. (New) An integrated circuit, comprising;

means for performing functions associated with a programmable logic core; and

means for performing functions associated with application specific circuitry that is designed in accordance with a sign-off design.

17. (New) An integrated circuit, comprising:

(I) application specific circuitry, the application specific circuitry being designed in accordance with a sign-off design; and

(II) a programmable logic core including at least

(A) a programmable multi-scale array having an array of configurable arithmetic logic units supporting register transfer level functions, random logic structures, and state machine structures,

(B) an application circuit interface for providing a signal interface between the programmable multi-scale array and the application specific circuitry, the application circuit interface having test registers for testing the programmable logic core,

(C) scratchpad memories for supplementing storage of the programmable multi-scale array,

(D) a configuration test interface for data and control flow between the application specific circuit and the programmable multi-scale array,

(E) a programmable logic control for loading configuration data into the multi-scale array, and

(F) a programmable logic core adapter that configures the programmable multi-scale array through the configuration test interface.

18. (New) A portion of programmable logic program flow comprising:

synthesizing data associated with a multi-scalable array and a program logic core design;

performing a programmable logic core mapping;

performing a programmable logic core placement;

performing a programmable logic core routing; and

performing a timing and netlist verification.